IARJSET
ISSN (Online) 2393-8021
ISSN (Print) 2394-1588
International Advanced Research Journal in Science, Engineering and Technology
ISO 3297:2007 Certified
Vol. 3, Issue 9, September 2016

Implementation of High Speed 32- Bit Carry Skip Adder Using Concatenation and Incremination Logic

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Abstract: In this paper, we present a carry skip adder (CSKA) structure that has a higher speed yet lower energy consumption compared with the conventional one. The speed enhancement is achieved by applying concatenation and incremination schemes to improve the efficiency of the conventional CSKA (Conv-CSKA) structure. In addition, instead of utilizing multiplexer logic, the proposed structure makes use of AND-OR-Invert (AOI) and OR-AND-Invert (OAI) compound gates for the skip logic. The structure may be realized with both fixed stage size and variable stage size styles, wherein the latter further improves the speed and energy parameters of the adder. The speed improvement was achieved by using variable size blocks; parallel prefix adders in the nucleus stage finally, a hybrid variable latency extension of the proposed structure, which lowers the power consumption without considerably impacting the speed. CI-CSKA has been synthesized using the XILINX ISE DESIGN SUITE 14.3 tool for Spartan3E family, the XC3S500E device with a speed grade of -5. Simulations on the variable latency CSKA show on average of 40% improvement in the delay.

Keywords: Carry skips adder (CSKA), energy efficient, high performance, hybrid variable latency adders, concatenation and incrementation (CI-CSKA).

I. INTRODUCTION

Adders are the basic building blocks of arithmetic logic units. Increasing the speed, reducing the energy consumption of adder can improve the performance of microprocessors. . In general, adders are generally found in the microprocessor designs, ALUs and Digital Signal Processing chips. Binary adders are extremely important not only for addition but also for Multiplication, subtraction, and division. A fast and correct operation of the digital system is more influenced by the performance of the adders. RCA has the simplest structure with the smallest area and power consumption but with the worst critical path delay. In the CSLA, the speed, power consumption, and area usages are considerably larger than those of the RCA.

The PPAs, which are also called carry look-ahead adders, exploit direct parallel prefix structures to generate the carry as fast as possible. There are different types of the parallel prefix algorithms that lead to different PPA structures with different performances. As an example, the Kogge-Stone adder (KSA) is one of the fastest structures but results in large power consumption and area usage. It should be noted that the structure complexities of PPAs are higher than those of other adder schemes One of the foremost effective adder structure in terms of area and power dissipation is that the carry-skip adder (CSKA). In fact, its speed is higher than Ripple carry adder (RCA) whereas being nearly equivalent in terms of area and power dissipation. Characterized by a good efficiency in the trade-off between power dissipation and speed since it has a lesser power-delay product, equivalent to that of a carry-look-ahead adder.

II. CONVENTIONAL CARRY SKIP ADDER

The carry skip adder consists of blocks of RCA 2:1 multiplexer for selection of carry.RCA consist of chain of full adder. Consider that A_i, B_i are the inputs to the full adder. The propagate signal P_i is given by

$$P_i = A_i \oplus B_i \quad \text{Where (i=1, 2.....N).}$$

Suppose consider N-bit carry skip adder consist of Q stages, each consist of M full adders the no. of stages is given by Q = $\frac{N}{M}$ .if Carry propagate (CP) equals to one in a particular stage then C_{OUT} of that is nothing but C_{IN} of that stage. If CP is equals to zero the delay is similar to Ripple carry adder. The 2: l multiplexer used for selection of Carry.

In each stage inputs to the 2:1 multiplexer are the carry input of that stage and carry out of particular RCA block. If carry propagate (CP) is zero the delay is similar to RCA.

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The block diagram of conventional CSKA shown below fig.1. The CSKA can be implemented with either fixed size stages (FSS) or variable size stages (VSS). The speed of CSKA can be increased by using variable size stages.

The critical path of the CSKA has three parts: 1) the path of the FA chain of the first stage it's delay is equal to M × T_{CARRY} ; 2) the path of the intermediate carry skip multiplexer it's delay is equal to the (Q – 1) × T_{MUX} ; and 3) the path of the FA chain in the last stage its delay is equal to the (M −1) × T_{CARRY} + T_{SUM} . T_{SUM} and T_{MUX} are the propagation delays of the carry output of an FA, the sum output of an FA, and the output delay of a 2:1 multiplexer, respectively. Hence, the critical path delay of a FSS CSKA is formulated by

$$T_D = [M \times T_{CARRY}] + \left[\left(\frac{N}{M} - 1\right) \times T_{MUX}\right] + [(M - 1) \times T_{CARRY} + T_{SUM}]$$

In the conventional CSKA, the delay is similar RCA if carry propagate is zero. This can overcome by using proposed structure.

III. PROPOSED CSKA STRUCTURE

A. Concatenation-Incrementation Carry Skip Adder:

The proposed CSKA structure consist of a concatenation and incrementation blocks in addition to conventional CSKA structure. The compound AOI, OAI gates are used instead of 2:1 multiplexer. AOI, OAI compound gates occupies less area. Compound gates are used for selection of carry. As the carry propagates through the skip logics, it becomes complemented.

Therefore, at the output of the skip logic of even stages, the complement of the carry is generated. The structure has a considerable less propagation delay with a slightly smaller area compared with those of the traditional one. Note that while the power consumptions of the AOI (or OAI) gate are smaller than that of the multiplexer, the power consumption of the proposed.

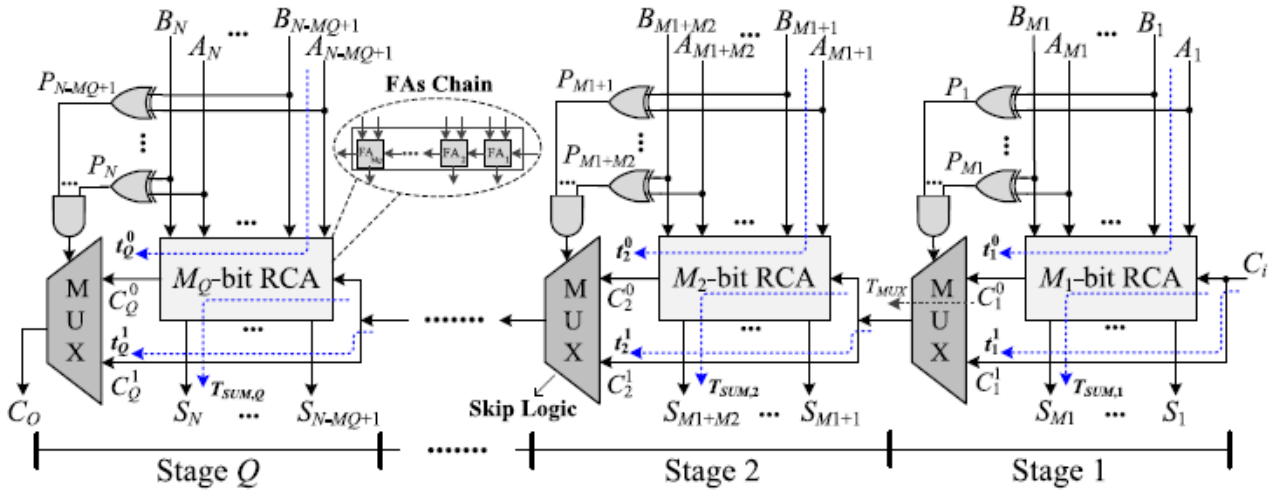

Fig.1 Coventional Carry Skip Adder

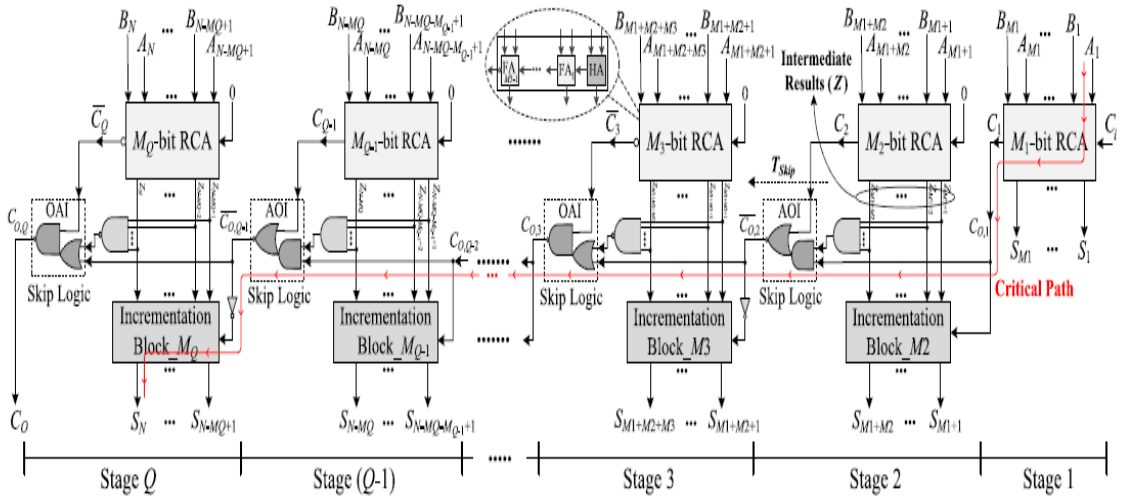

Fig.2 Proposed CI-CSKA structure

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CI-CSKA is a little higher than that of the conventional one. This is due to the increase in the number of the gates, which causes a higher wiring capacitance (in the noncritical paths).the block diagram of proposed CSKA structure shown below. Now, we describe the internal structure of the proposed CI-CSKA shown in Fig. 2 in more detail. The adder contains two N bits inputs, A and B, and Q stages. Each stage consists of an RCA block with the size M_j (j=1, 2 ...Q) in this structure all the stages provided with carry input is '0', except first stage. Therefore all sums are generated simultaneously. The proposed CSKA structure, first stage consists of single block of RCA. The remaining blocks from 2 to Q consist of block of RCA incrementation logic. Intermediate results generated by the RCA block and the carry output of the previous stage to calculate the final summation of the stage.

B. Area and Delay of the Proposed Structure:

The use of the static AOI and OAI gates (six transistors) compared with the static 2:1 multiplexer (12transistors), leads to decreases in the area usage and delay of the skip logic. In addition, except for the first RCA block, the carry input for all other blocks is zero, and hence, for these blocks, the first adder cell in the RCA chain is a HA. This means that (Q − 1) FAs in the conventional structure are replaced with the same number of HAs in the suggested structure decreasing the area usage.

In addition, note that the proposed structure utilizes incrementation blocks that do not exist in the conventional one. These blocks, however, may be implemented with about the same logic gates (XOR and AND gates) as those used for generating the select signal of the multiplexer in the conventional structure. Therefore, the area usage of the proposed CI-CSKA structure is decreased compared with that of the conventional one.

The critical path of the proposed CI-CSKA structure, which contains three parts, is shown in Fig. 2. These parts include the chain of the FAs of the first stage, the path of the skip logics, and the incrementation block in the last stage. The delay of this path (TD) may be expressed as

$$T_D = [M_1 T_{CARRY}] + [(Q-2)T_{SKIP}] + [(M_Q - 1)T_{AND} + T_{XOR}]$$

Where the three brackets correspond to the three parts mentioned above, respectively. Here, T_{AND} and T_{XOR} are the delays of the two inputs static AND and XOR gates, respectively.

C. Incrementation logic:

The internal structure of the incrementation block, which contains a chain of half-adders (HAs), the incrementation block use the intermediate results generated by the RCA block and the carry output of the previous stage to calculate the final summation of the stage. The internal structure of the incrementation block, which contains a chain of half-adders (HAs), is In addition note that, to reduce the delay considerably, for computing the carry output of the stage, the carry output of the incrementation block is not used. The block diagram of incrementation logic shown below

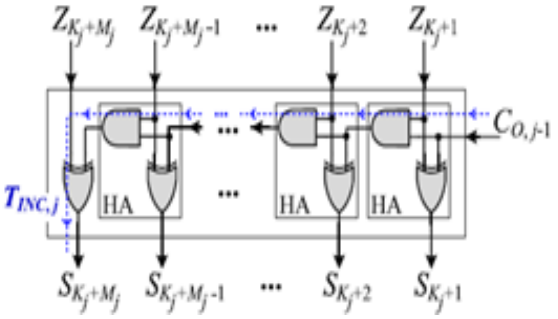

Fig. 3 Internal structure of the incrementation block

The output carry of j^{th} was identified by intermediate results of j^{th} stage and carry out of previous stage and carry out of RCA block. If the product of intermediate results is '1' carry out of RCA block equals to carry in of that stage. The reason for using both AOI and OAI compound gates as the skip logics is the inverting functions of these gates in standard cell libraries. This way the need for an inverter gate, which increases the power consumption and delay, is eliminated. If an AOI is used as the skip logic, the next skip logic should use OAI gate. The delay is further reduced by using variable size stages instead of fixed size stages. The speed of CI-CSKA further improved by using parallel prefix adders in nucleus stage.

IV. RESULTS AND DISCUSSIONS

Different adder structures are coded using VHDL. The synthesis was performed using the XILINX ISE DESIGN SUITE 14.3 tool for Spartan 3E family, the XC3S500E device with a speed grade of -4.The performance comparison of different adder structures with reference to delay is given in Table-I for 16bit width and Table-II for 32-bit width.

Table -I Performance Analysis of Various Adders of 16-bit width

Different adder structure	Delay(ns)
RCA	24.776
Conventional CSKA	21.690
CI-CSKA	19.046
Variable size CI-CSKA	17.40

Table -II Performance Analysis of Various Adders of 32-bit width

Different adder structure	Delay(ns)
RCA	38.665
Conventional CSKA	33.917
CI-CSKA	22.07
Variable size CI-CSKA	20.07

DOI 10.17148/IARJSET.2016.3938

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From the above performance analysis tables, we will conclude that CI-CSKA has less delay when compared with conventional CSKA and other adder structures. Hence, it can be used for high-speed applications.

Simulation results:

Using ModelSim software the output analysis of Concatenation-Incrementation Carry Skip Adder with 32-bit width was obtained and it is shown in below figure 4.

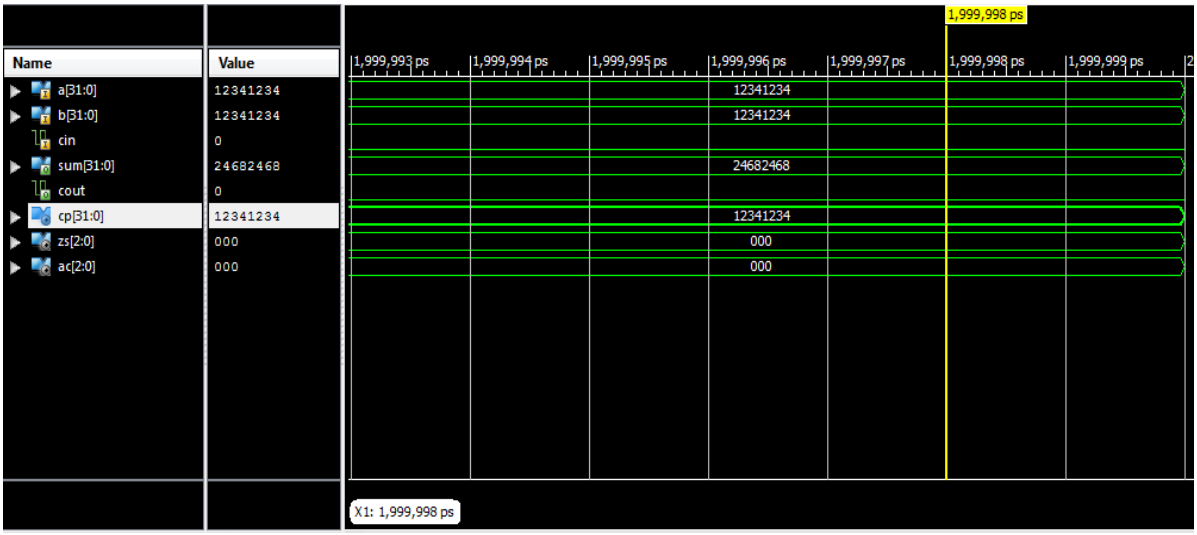

Fig. 4 Simulation results for 32-bit input proposes carry skip adder

V. CONCLUSION

In this paper, an improved speed CSKA known as Concatenation-Incrementation CSKA (CI-CSKA) has been proposed. The CI-CSKA exhibits a higher speed compared with those of the Conventional one.

Moreover, the speed enhancement is achieved by using concatenation and Efficiency is improved by incrementation schemes. In addition, AND-OR-Invert and OR-AND-Invert compound gates were employed for the carry skip logic. A variable latency extension of the CI-CSKA structure was proposed.

The efficiency of the variable latency extension structure was studied by comparing its delay with those of the Traditional CSKA, RCA, CI-CSKA, and Brent-Kung adder structures. The results indicates much lower propagation delay for CI-CSKA when compared with conventional CSKA .the speed is further increased by using variable size stages, parallel prefix adders in nuclear stage. CI- Carry Skip Adder structure is the best adder for high-speed applications.

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BIOGRAPHIES

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